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10/674,085	09/29/2003	Elias Fallon	188122003600	2168

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EXAMINER	
ROSSOSHEK, YELENA	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 11/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/674,085	FALLON ET AL.	
	Examiner	Art Unit	
	Helen Rossoshek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17,24,25,27-30 and 34-36* is/are rejected.

7)☒ Claim(s) *18-23,26,31-33,37 and 38* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/4/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the Application 10/674,085 filed 09/29/2003.

2. Claims 1-38 are pending in the Application.

Claim Objections

3. Claim 19 is objected to because of the following informalities:

There is insufficient antecedent basis for the limitation "the component associated with each . . ." in the claim 19.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. Claims 4 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The omitted structural cooperative relationships are: it is not clear what relationship between positions of the components on the tree structure and global symmetry line since claim 4 extents the step c) of the claim 1.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States

only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1-17, 24, 25, 27-30, 34-36 are rejected under 35 U.S.C. 102(e) as being anticipated by Hassibi et al. (US Patent Application Publication 20020184603).

With respect to claims 1, 24, 34, 35 and Hassibi et al. teaches a computer-implemented method for determining component placement in a circuit within computer aided design system for the design, optimizing and floorplanning of integrated circuit (abstract; paragraph [0015]), a computer readable medium having stored thereon instructions which, when executed by a processor, cause the processor to perform the steps (paragraph [0015]): (a) receiving a plurality of components, with each component having associated therewith a width, a height and one of a symmetric and a non-symmetric placement constraint as shown on the Figs. 3 and 4 wherein plurality of components are depicted, such as transistors M_1, M_2, M_3 etc. (paragraph [0023]), each having dimensions as width, height (paragraph [0022]) and placed on the floorplan by linear equality constraints (symmetric) and inequalities constraints (non-symmetric) as polynomial constraints (paragraph 0015]); (b) creating a tree structure that expresses the placement constraints for the plurality of components as shown on the Fig. 5, which represents the floorplan of the components depicted on the Fig. 4 (paragraph [0026]), the tree structure including: a global root node that represents a global symmetry line as shown on the Fig. 5 the line beginning at node 0 by the line 51 (paragraph [0026]), a leaf representing each component, with the component associated with each leaf tagged for placement on a first side, a second side, or on both sides of the global symmetry line, and at least one interior node that represents a slicing line that

establishes a relative placement of at least two components with respect to each other on the same side of the global symmetry line as shown on the Fig. 5 including leafs as nodes representing the components of the integrated circuit represented on the Fig. 3 which are located on one or both sides of the global line and having slice lines as interior nodes (paragraphs [0027], [0028], [0029]); (c) performing at least one structured search of the tree structure to determine the initial placement of components on the first side, the second side or both sides of the global symmetry line based on the tagging of each component and the connections of the leaves, the global root node and the interior nodes to form the tree structures as shown on the Fig. 5 given the slicing tree, wherein slicing is continues until the entire circuit is sliced into individual cells for which the boundaries are to be determined (paragraph [0033]); and (d) performing another structured search of the tree structure to determine the final placement of components based on at least one of the widths and heights of the components as shown on the Figs. 6 and 7 for illustrating another example of circuit floorplan and slicing tree (paragraph 0046]), wherein for the slicing process the algorithm presented on the Fig. 2 is used (paragraph 0042]).

With respect to claim 27 and 36 Hassibi et al. teaches a computer-implemented method for determining component placement in a circuit; a computer readable medium having stored thereon instructions which, when executed by a processor, cause the processor to perform the steps within computer aided design system for the design, optimizing and floorplanning of integrated circuit (abstract; paragraph [0015]), comprising: (a) forming in the memory of the computer a tree structure that defines the

placement of each of a plurality of components associated with the tree structure on a first side, a second side, or symmetrically on both sides of a symmetry line, with at least one component tagged for symmetric placement on both sides of a symmetry line as shown on the Figs. 3 and 4 wherein plurality of components are depicted, such as transistors M_1, M_2, M_3 etc. (paragraph [0023]), each having dimensions as width, height (paragraph [0022]) and placed on the floorplan by linear equality constraints (symmetric) and inequalities constraints (non-symmetric) as polynomial constraints (paragraph 0015]), wherein computer aided design (CAD) technique using the concept of dimensional constraints such as symmetry and matching is improved and used for the designing integrated circuit relied upon geometric programming (paragraphs [0002], [0003]); (b) performing at least one search of the tree structure to determine an initial placement of a subset of the components on the first side, the second side, or on both sides of the symmetry line as shown on the Fig. 5 given the slicing tree, wherein slicing is continues until the entire circuit is sliced into individual cells for which the boundaries are to be determined (paragraph [0033]); and (c) performing another search of the tree structure to determine a final placement of the subset of components, wherein at least a part of each component tagged for symmetric placement is positioned on each side of the symmetry line as shown on the Figs. 6 and 7 for illustrating another example of circuit floorplan and slicing tree (paragraph 0046]), wherein for the slicing process the algorithm presented on the Fig. 2 is used (paragraph 0042]).

With respect to claims 2-17, 25, 28-30 Hassibi et al. teaches:

Claims 2, 28: each structured search is a depth-first search within the geometric programming relying on the abilities of programming attributes (paragraph [0002]);

Claims 3, 29: each slicing line has a direction that is one of parallel and perpendicular to the global symmetry line as shown on the Fig. 5 presenting the slicing lines as vertical along the global slicing line or horizontal as perpendicular to the global slicing line (paragraphs [0028], [0029]); and step (c) includes the placement of the at least two components with respect to each other as a function of the direction of the slicing line (paragraph [0032]);

Claim 4: step (c) includes, for components tagged for placement on the same side of the global symmetry line, placing a component associated with a leaf positioned lower in the tree structure closer to the global symmetry line than a component associated with a leaf positioned higher in the tree structure within consideration of the horizontal and vertical dimensions of the components placed on the structure of the slicing tree (paragraph [0030]);

Claim 5: each node has a pair of branches descending therefrom; and each branch couples the node from which it descends to (1) one of the interior nodes, (2) one of the leaves, or (3) a null as shown on the Figs. 5 and 7, wherein each branch might have a node, a leaf or nothing in the end of the tree depending on the scheme of the integrated circuit shown on the Fig. 4, for which the slicing tree is structured;

Claim 6: step (c) includes, for an interior node that represents a slicing line that is parallel to the global symmetry line: placing on one side of the global symmetry line, a first component which is tagged for such placement and which is represented by a leaf

which is connected to the interior node via one of its branches as shown on the Fig. 5 such as component C_c which is placed on one side of the global symmetry line according to the Fig. 4; and placing on a side of the first component opposite the global symmetry line a second component which is tagged for placement on the one side of the global symmetry line and which is represented by a leaf which is connected to the interior node via the other of its branches as shown on the Fig. 5 such as component M_2, which is placed on the opposite side of the symmetry line from the first component C_c;

Claim 7: at least one of the leaves representing the first and the second components is connected directly to the interior node as shown on the Fig. 5 such as components M_5 and M_6 which are connected to the interior node 3 from the Fig. 4;

Claim 8: (c) includes, for the global root node: placing a first component which is tagged for placement on one side of the global symmetry line and which is represented by a leaf which is connected to the global root node via one of its branches as component C_c as shown on the Fig. 5; and placing on a side of the first component opposite the global symmetry line, a second component which is tagged for placement on the one side of the global symmetry line and which is represented by a leaf which is connected to the global root node via the other of its branches as component M_2 from the Fig. 5;

Claim 9: at least one of the leaves representing the first and second components is connected directly to the global root node such as components M_4 and C_c connected to the global root 0;

Claim 10: step (c) includes, for an interior node that represents a slicing line that is perpendicular to the global symmetry line: placing on one side of the global symmetry line, a first component which is tagged for such placement and which is represented by a leaf which is connected to the interior node via one branch descending therefrom as component C_c as shown on the Fig. 5; and placing one of above and below the first component, a second component which is tagged for placement on the one side of the global symmetry line and which is represented by a leaf which is connected to the interior node via the other branch descending therefrom as component M_2 as shown on the Fig. 5;

Claim 11: step (d) includes placing one edge of a component adjacent the global symmetry line when the leaf representing the component is one of: connected to a node at the lowest level of the tree structure via one branch descending from the node; or connected to the node via the other branch descending therefrom and no other leaf is connected to the interior node via the one branch descending therefrom as shown on the Fig. 7 (paragraph [0041]);

Claim 12: for each component tagged for placement on both sides of the global symmetry line in a pair-symmetric manner, step (c) includes placing first and second copies of the component on the respective first and second sides of the global symmetry line, with each copy of the component having a side closest to the global symmetry line positioned a distance D therefrom (paragraph [0056]);

Claim 13: the distance D is one of: zero when the leaf representing the component tagged for pair-symmetric placement is connected directly to a node at the

lowest level of the tree structure; or the greater of (1) a sum of the width(s) or height(s) of each component placed on the first side of the global symmetry line prior to placement of copies of the component tagged for pair-symmetric placement or (2) a sum of the width(s) or height(s) of each component placed on the second side of the global symmetry line prior to placement of copies of the component tagged for pair-symmetric placement (paragraph [0033]);

Claim 14: for each component tagged for placement on both sides of the global symmetry line in a self-symmetric or asymmetric manner, step (c) includes placing a first part of the component on the first side of the global symmetry line and placing a second part of the component on the second side of the global symmetry line (paragraphs [0015], [0056]);

Claim 15: for each component tagged for self-symmetric placement, the first part of the component is one-half of the component and the second part of the component is the other half of the component within slicing proportion depends on the sizing of the components as variables x and y representing the height and width of the components, wherein the symmetrical slicing slices in two halves using linear equality constraints (paragraph 0015]); and for each component tagged for asymmetric placement, the first part of the component is a first percentage of the component, the second part of the component is a second percentage of the component, and the sum of the first and second percentages equal one-hundred percent within slicing by inequality constraints (paragraphs [0030], [0031]);

Claim 16: for each component tagged for offset symmetric placement on one side of the global symmetry line a distance D from the global symmetry line, step (c) includes placing the component on the one side of the global symmetry line with the side of the component in opposition with the global symmetry line positioned the distance D from the global symmetry line as shown on the Fig. 5 (paragraphs [0026]-[0029]);

Claim 17: defining an isolation structure along at least one side of at least one component; and in step (d), placing the one side of the at least one component no closer to another component or the global symmetry line than the isolation structure within consideration of the electrical specifications (electrical/isolation constraints) including step 25 of the Fig. 2 (paragraph [0025]);

Claim 25: performing at least one structured search of the tree structure to determine the initial placement of the group tree structure on the first side, the second side or both sides of the global symmetry line based on the tagging of the group tree structure as shown on the Fig. 5 given the slicing tree, wherein slicing is continues until the entire circuit is sliced into individual cells for which the boundaries are to be determined (paragraph [0033]); and performing another structured search of the tree structure to determine the final placement of the group tree structure (paragraph [0033]);

Claim 30: the symmetric placement includes one of: pair-symmetric placement using linear equality constraints (paragraph [0015]); self-symmetric placement

(paragraph [0056]); and asymmetric placement using inequalities constraints (paragraph [0015]).

Allowable Subject Matter

7. Claims 18, 31-33, 37, 38 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The prior art of record does not teach exchanging the location of two components in the tree structure; exchanging the location of one leaf and one interior node and any interior node and/or leaf connected to the interior node; exchanging the width and height of a component associated with at least one leaf while symmetrical and non-symmetrical constraints are used as claimed.

8. Claims 19-23 have allowable subject matter: grouping tree structure including group which is tagged for placement on the first side, the second side, or both sides of the global symmetry line, wherein the component associated with each leaf of the group tree structure is tagged for placement on the first side, a second side, or on both sides of the local symmetry line as claimed.

9. Claim 26 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The prior art of record does not teach substituting the final placement of the components of a group tree structure for the final placement of the group tree structure while symmetrical and non-symmetrical constraints are used as claimed

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Helen Rossoshek whose telephone number is 571-272-1905. The examiner can normally be reached on 7:00-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Examiner
Helen Rossoshek
AU 2825

A. M. Thompson
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Technology Center 2800